Investigating Carbon Nanotube Field-effect Transistors to Use in Adder Circuits

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Abstract—**In recent decades, the attempt to perform more computational and processing operations on a silicon chip using adders has created a strong desire to reduce the circuit components scale, especially transistors. Speed and power consumption constraints also push designers to utilize smaller dimensions. There were some problems to reach transistors with smaller dimensions. One of the reasons was due to the employing of silicon dioxide SiO_2 as insulation. The over-thinning of this material in the transistors dimension reduction process caused a great loss of energy, current leakage, and chip over-heating during operations. Ultimately, the goal of reducing dimensions is to build a transistor that is smaller, faster, cheaper, and less power consuming. After many experiments, researchers concluded that carbon nanotubes, which are based on carbon structures, could replace the old silicon structure. They concluded that transforming graphene into graphene nano-bars, and limiting electron in a particular direction may create an energy gap in the graphene. The previous research outcomes show that using carbon nanotubes results in delay and power consumption reduction, which in turn decrease the delay and power product. The results of research across all adders with carbon nanotube design show a significant improvement in power and delay parameters compared to previous designs with MOSFET. For this purpose, in this paper, we presented a general overview of transistors which play an important role in reducing the dimensions and delay and power product improvement with proper performance and low power consumption for adders.**

***Index Terms*— carbon nanotube field-effect transistors, adders, CNTEFET**

I. INTRODUCTION

SO FAR, different structures have been proposed for carbon nanotube transistors, while each one has its own characteristics and is suitable for specified applications. For example, devices with thin film (a network of nanotubes) are more suitable to employ as a channel in flexible and transparent electronic devices.

One of desired characteristics for transistors applications is the high mutual conductivity, which naturally may obtain in the structures in which the gate control is higher over the channel. For example, a coaxial gate structure can address this requirement. Another suitable feature is the transistor high ON mode current, to achieve that, a structure that uses an array of carbon nanotubes as a channel is appropriate [1] [9]. In 1930, Lilienfeld introduced the initial concept of a field-effect transistor. Thirty years later, in 1960, the first sample was realized using Si-SiO_2 by Kahng and Atalla. Since then, field effects transistors have been embedded in integrated circuits and have grown to become the most important technology in the electronics industry. For nearly half a century, the number of transistors in integrated circuits doubled approximately every 18 to 24 months, which in 1965 Gordon Moore referred to this trend for the first time. This trend that has followed an exponential behavior is well-known as Moore's law. Moore examines the components number and construction cost for integrated circuits, and concludes that at any time, the common technology has a minimum cost, and this minimum is decreasing with time, while the number of components in the integrated circuit in these minimums is increasing [1].

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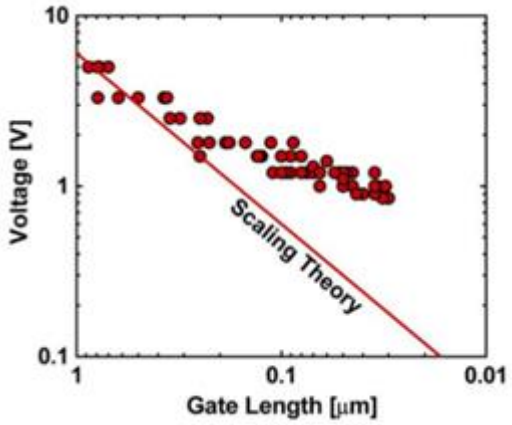
In 1974, Robert Dennard proposed a method to scale the MOSFET dimension, which provides a simple approach to design the next generation of smaller scale MOSFET devices. According to this theory, it is possible to apply an appropriate coefficient to scale the technology parameters, keep its inward electric field constant while the chip dimensions are decreasing [15] [7] [2]. This solution increases the device's stability against the channel effect and its reliability, and more importantly, it improves the circuit's delay without increasing the power density. Upon reaching the sub-micron dimensions, the base forces changed the scale rules. In particular, due to the voltage threshold non-scalability, the voltage source scaling was slowed down and appeared to be an obstacle to control power leakage in recent years. Sub-threshold leakage (sub-threshold conduction of gate oxide leakage and reverse bias leakage), which was previously neglected, consumes up to half of the total power consumption in modern chips. In addition, considering that the power supply is not reduced with all dimensions. The power density increases during the time, which means generating more heat in the circuit.

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

κ is the dimensional scale factor

(a)



(b)

Fig.2: a) Scale theory to keep electrical field constant in a MOSFET device. b) Scale trend in voltage sources in CMOS technology. With regards to the voltage levels leakage, they are become extremely distant to the scale theory with constant field [3].

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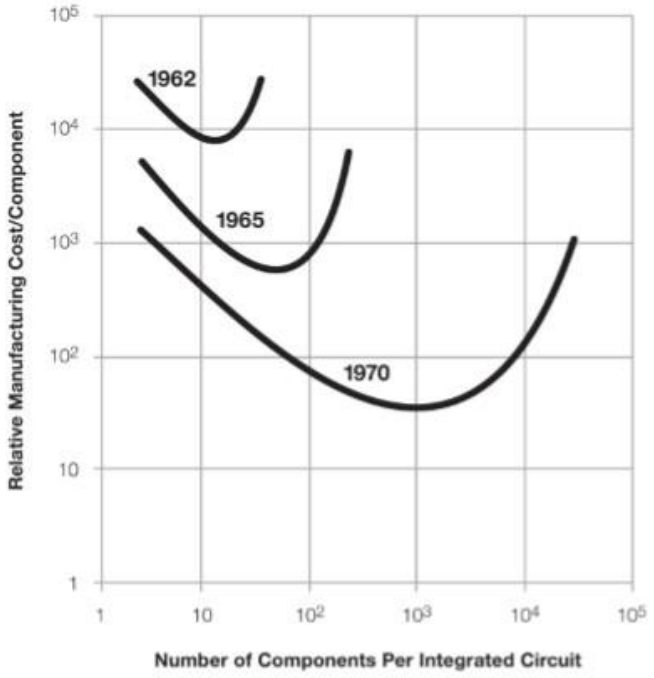
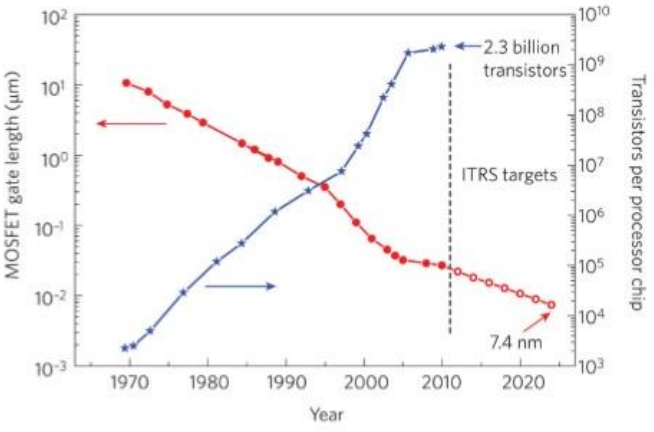


(a)



(b)

Fig.1 a) Relative construction cost per components number in the integrated circuit b) MOSFET gate length variation in the integrated circuit construction stage (bold red circles) and ITRS goals (hollow red circles) increase with reduction of transistors number gate length for each processing chip (blue stars).

As the MOSFET becomes smaller, the number of atoms in silicon decreases, which determines many features of transistors. Consequently, controlling the number of impurities and their placement may include more errors. Modern integrated circuits are simulated using computers so that the circuits that work properly are obtained from the first generation. Shrinking the chip results in more difficulty in precision process complexity, and physical processes modeling becomes more challenging. As a result, sufficient simulation is difficult for the first generation [13].

II. RELATED WORKS

Over the past two decades, the complementary metal-oxide semiconductor technology (CMOS) has become increasingly important across integrated circuits industry. Although the bipolar and silicon devices, and the III-V group still have their own proper applications, today only CMOS processes are becoming a successful choice for integrating digital and analog circuits. But in the last decade, this is done using nano-scale transistors due to scalability limitation (short-channel effects), including leakage current caused by deep-submicron technology [2], such as carbon nanotubes. These transistors do not have a leakage current like MOSFET, but suffer from a disturbing current called band to band tunneling (BTBT) [3]. The CNTFET transistor is suitable for implementing logic circuits because of its high performance and low power consumption [4].

To simulate the CNTFET field effect transistor, it is necessary to model current-voltage equations (I-V) in order to understand the dc and capacitance-voltage equations (C-V) behavior to predict ac characteristics. In compact models reported to date, most of the proposed models in [5] and [6] are numerical and

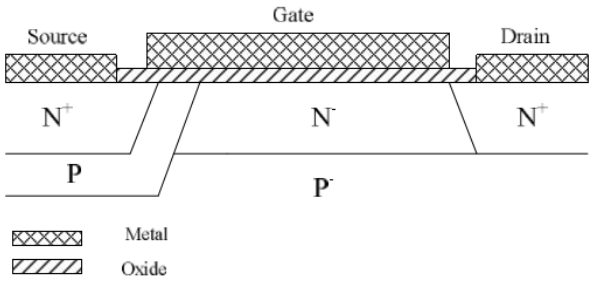


Fig 4: The structure of horizontal DMOS transistor.

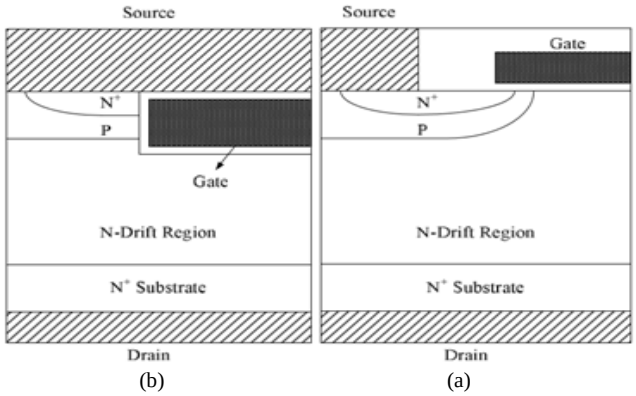


Fig 5: a) Vertical D-MOS transistor b) U-MOS transistor.

require intensive computational effort, resulting in more

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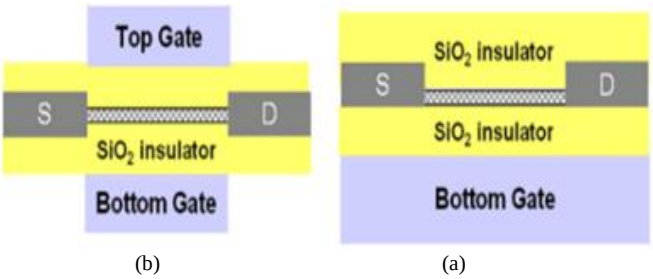
difficulty for implementation in SPICE-based circuit simulators. Also, an ideal ballistic is used for device modeling. This simplification creates questions when the device transient response and dynamic function are evaluating. The polynomial fitting approach that used to solve the integral significantly improves the execution time, but is not suitable for evaluating the CNT-MOSFET performance with different device parameters (such as CNT chirality, gate oxide thickness). A complete model is used in [3] and [4] to solve the integral of the summation function. By using the device complete model, the effects of chirality, channel length and nanotubes numbers could be found in CNTFET simulation, for both small signal (analog) and large signal (digital) applications. In this model, device non-idealities are also included, such as source/drain resistance, shotckey barrier resistance (SB), the charge screening effect between different nanotubes (center and side) and phonon scattering (acoustic and optical).

Typically, the digital circuits design with two logical levels of zero and one is performed in the binary space; however, it is possible to add several other logical levels to the binary logic, namely multiple valued-logic (MVL), and employ them in digital circuits design. By adding one and two logical levels to binary logic, the "ternary" and "quaternary" logics will be made respectively. Multiple valued-logic has different fields. Lukasia Vich [8] and Keliny [9] are the most famous ones in the multiple valued-logic fields. Keliny field is much known and accepted with respect to symbolic and suitable definitions that provided



(b) (a)

Fig 6: General schema a) graphene-based transistor with one gate b) graphene-based transistor with one gate [3].

for basic operators.

III. Various Types of Transistors

The overall view of the MOSFET transistor is shown in Fig. 3. This structure can withstand a small drain-source voltage. Therefore, this structure should be modified in power applications. As can be seen, the structure called double diffused MOS (DMOS) works for voltages of 10 volts and above. In this transistor, an n-type semiconductor area is created which causes the voltage to be blocked. The horizontal DMOS transistors (LDMOS) are in use across integrated power circuits, but these devices have drawbacks such as low flow rate, because the area n includes a large part of the semiconductor area.

The structure of n-type D-MOS vertical transistor, as shown in Fig. 5a, is created using the difference in the horizontal expansion of the bonds under the gate electrode. Another structure used in power applications is the U-MOSFET transistor which was commercially released in 1990. This transistor's gate structure is embedded [3], [6].

Therefore, with respect to the power transistors applications and

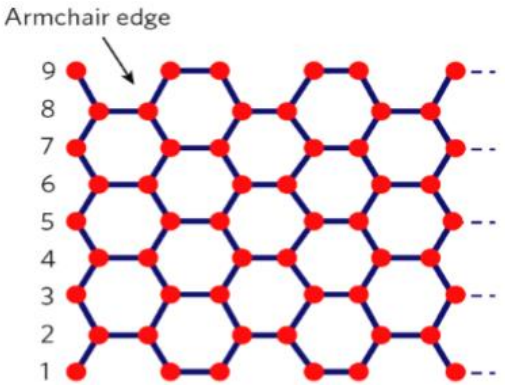


Fig 8: Armature graphene nanobar with numbering nanobar width atoms.

types, it is necessary to improve these devices characteristics.

A. Field effect transistor based on graphene nano-bar

In 1956, Gordon Moore, the founder of Intel, reported that the number of transistors used in Intel's microprocessors doubles every 18 months, while the transistors gate dimensions are halved due to the result of these rules, when the size of silicon chip is fixed. This law was called the Moore's law. This reduction by half actually represented the economic aspects, i.e. as the gate is smaller the transistor could switch faster, consequently, lower energy is consumed and more transistors are embedded in a silicon chip. But increasing the transistors number leads to an increase in temperature. In the meantime, the graphene material with unique properties that it exhibits was a good alternative to silicon technology [45].

The study of graphene field effect transistor began in 2004 with the discovery of the bipolar electric field effect by Novoslof and Gim. They showed that the properties of multi-layered graphene electrical are largely different from bulk graphite which has a three-dimensional structure. One of the most straightforward and important applications of graphene is its use as a transistor channel.

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The channel material in a field effect transistor could be single-layer graphene, two-layer or multi-layered graphene. The transistor performance is influenced by the number of graphene layers in the channel, because the electrical properties change from single-layer to the multi-layer. The number of layers could be extracted by Raman measurements.

Graphene with armature edges could exhibit semi-conducting and semi-metallic properties. The graphene nano-bar whose number of atoms within a nanotube is equal to 3k and 3k+1, has semiconductor properties, and the graphene nano-bar whose number of atoms in the nanotube is equal to 3k+2, has semi-metallic properties.

When the gate dielectric thickness decreases, the channel quantum capacitor must be considered. This capacitor results from the density of graphene states with the Fermi-Dirac distribution for load carriers and is almost linearly dependent on the channel voltage and has a minimum amount around the minimum conductivity point. In addition, the capacitance is symmetric with respect to the Dirac point and is affected by defects and impurities.
Ponomarenko et al. have made bars with a width of about 10 nm and an approximate gap of 500 mV, using a beam lithography method. The transistors off-mode resistance made up with these bars was not measurable at room temperature. Li et al. also made thin nanobars in a different way. The $\frac{I_{on}}{I_{off}}$ ratio of the transistors fabricated with these bars was very good and more than 10^6. The experimental $\frac{I_{on}}{I_{off}}$ ratios reported for the years 2007-2009 for graphene-based transistors are shown in the figure below.

B. *Carbon nanotube field transistor*

Carbon Nanotubes (CNT) are made of cylindrically rolled graphite sheets with various diameters. The CNT can be constructed either as a single-walled (SWCNT) or as a multi-walled (MWCNT). Depending on the angle at which the single-walled carbon nanotube is rolled, it is called a chirality vector and is represented by two integer pairs of m and n. The ratio of diameters based on the chirality coefficients for a single-walled carbon nanotube (SWCNT) is obtained from the following equation [16]:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + nm + m^2} \qquad (1)$$

Where $a_0 = 0.142$ nm is the interatomic distance between each carbon atom and its nearest neighbor.
The carbon nanotubes could be semiconductor depending on the diameters (chirality), provided that the difference in chirality coefficients n_1 and n_2 is divided into three non-zeroes; otherwise, the carbon nanotubes will be metallic. The energy gap for a carbon nanotube is dependent on the CNT diameter semi-conductivity. The minimum voltage required for a transistor to turn ON, called the threshold voltage, is half of the energy gap due to the channel intrinsic nature and the placement of a Fermi level in the middle of the bar [7]:

$$V_{TH} = \frac{E_G}{2e} = \frac{\sqrt{3}}{3e}\frac{a\,V_\pi}{D_{CNT}} \qquad (2)$$

Where e is the charge of an electron, a $= 2.49$ Å is the distance of carbon atom to the carbon, and $V_\pi = 3.033$ eV is the π-π bond energy in the tight bonding model.
This equation shows the relation of threshold to the nanotubes diameter. It is possible to use the threshold voltage dependency to the nanotubes diameter in the multi-value circuit design [4]. The threshold voltage is positive for n-type transistor and negative for p-type transistor. An example of a single-wall CNTFET transistor with four identical nanotubes is shown in the figure below. A compact model related to this device has been published in [8] and [9], which both codes based on HSPICE and Verilog-A are provided in the site. This model is designed for CNT-MOSFET, which has a unipolar behavior. Using this compact model enables simulation on both device and circuit levels.

IV. An Overview of the Previous Designs for a Full Adder with CNFET Technology

A. *Parallel prefix adder*

According to the all abovementioned points, in this section we provide a parallel prefix adder circuit which is more optimal in terms of circuit parameters compared with other items provided in this regard, such as speed and power consumption. This adder is implemented using CNTFETs and the AND\OR\XOR

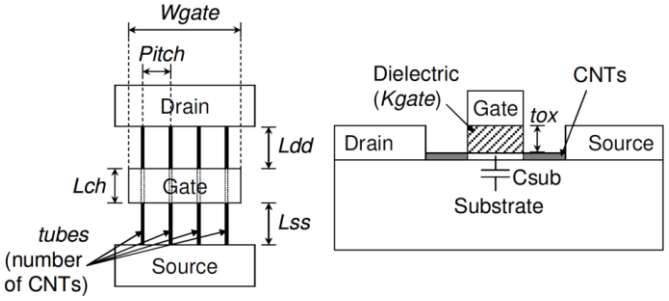

Fig 10: Side and top view of CNTFET transistor [5].

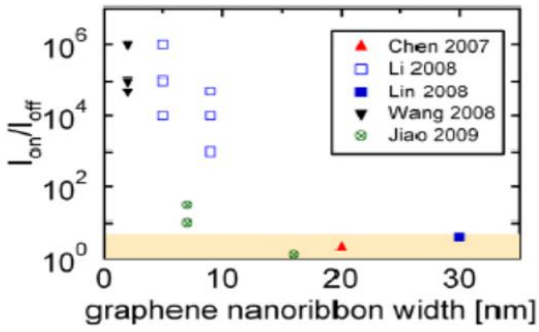

Fig 9: $\frac{I_{on}}{I_{off}}$ ratios per bars width which are obtained experimentally [11].

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gates are used in its internal structure. Prefix adders are a derivative of carry prediction adders. The prefix adder can be implemented using the following relationships.

$$A = (An\text{-}1 \ldots A2\ A1\ A0)$$
$$B = (Bn\text{-}1 \ldots B2\ B1\ B0)$$
$$S = (Sn\text{-}1 \ldots S2\ S1\ S0) \quad , \quad S = A + B$$
$$P = (Pn\text{-}1 \ldots P2\ P1\ P0) \quad , \quad Pi = Ai \oplus Bi$$
$$G = (Gn\text{-}1 \ldots G2\ G1\ G0) \quad , \quad Gi = Ai \,.\, Bi$$
$$Ci = Gi\text{-}1 + Pi\text{-}1 \,.\, Ci\text{-}1$$
$$Si = Ci \oplus Pi$$

In this adder, we assign the input bits to two different blocks and get the (P, G) outputs from them. The goal is to convert two blocks into a single block, and the blocks position should not be changed, because the carry is transferred from the right side block to the left side block. As shown in the figure below, all the circuit inputs and outputs are 2-bit, and they have two modes

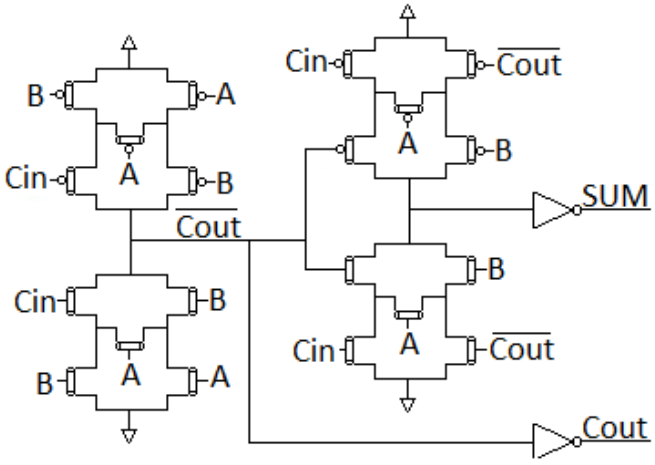

Fig 13: full adder circuit based on carbon nanotubes

that generate either a carry or transfer the previous step carry as shown in the figure below:

In the second case, the right-side block and the entire block has only one output and is single-bit, and only the left-side block has two outputs and is 2-bit. The carry goes to the next category according to the following relation:

B. Full adder using carbon nanotube field effect transistors with full transistor structure

Capacitors and resistors are considered to be destructive elements in the circuits design and cause the power consumption, delay and product of these two values and in general all of the circuit parameters be out of optimal mode, so it is better these elements not be used in the design as much as possible. In this paper, a full adder is presented using carbon nanotubes field effect transistors. In this design, we used 24 CNTFET transistors, without using any resistive and capacitive elements.

Figure 13 shows the full adder circuit at the transistor level [10].

V. CONCLUSION

In this paper, we examined carbon nanotube based nano circuits. Carbon nanotubes are one of the best choices for replacing silicon-based technology over the coming years due to their excellent electrical characteristics. Because of very small dimensions in carbon nanotubes technology, the reliability and efficiency of the circuits which are based on this technology are among the most controversial issues ahead of this technology. Hence, providing a method to improve these two parameters in carbon nanotubes technology is of great importance. We can achieve an improved technology in terms of power consumption and delay by providing improved methods to generalize the variant gates designs with more transistors with the help of CNFET technology across various logic circuits, such as multiplexers and decoders.

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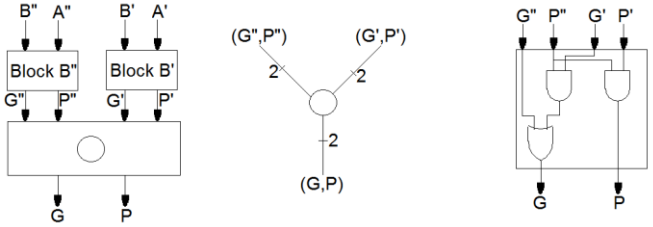

Fig 11: 2-bit (G, P) generator

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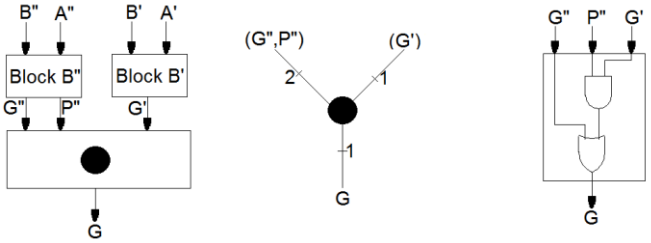

Fig 12: 1-bit (G, P) generator

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