Design of a new full_ Adder using silicon transistors

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Abstract— The collectors are one of the most important elements in digital circuits. Providing an optimal design of this element will significantly help improve the output parameters of these circuits a new design of all collectors is presented using transient gate transistor The simulation results obtained using the HSPICE software at a voltage of 1.8 volts are presented below. Simulation results show a significant improvement in power parameters, latency and previous designs.

***Index Terms*—:**Full Adder, gate transistor**,.**

I. INTRODUCTION

The latency of circuits designed with silicon transistors due to the use of intermediate capacitors in the integrated circuits is very large and this results in a decrease in the efficiency of the whole circuit. Given the fact that the circuitry used in the design of the capacitors, because of the low ability of the gate to drive capacitive loads, the circuits speed is noticeably reduced, and this is one of the problems with the design of integrated circuits with silicon transistors. Collectors are one of the most important elements in digital circuits. Therefore, providing an optimal design of this element will significantly help improve the output parameters of these circuits.

All collectors are implemented using equation (1)

$$SUM = A \oplus B \oplus CIN \qquad (1)$$
$$COUT = A.B + CIN\ (A \oplus B)$$

II. PREVIOUS DESIGNS

many CMOS collectors have been provided. One of the first all collectors with 24 transistors is provided with 26 transistors bridge and all the next collector And is implemented symmetrically . in 24 compared to the one with lower power consumption, which is less because of the number of transistors, but because the output of the sum24 transistor circuit sum is smaller but due to the output One must wait for the output, so the circuit is delayed24 more than the 26th circuit should wait for the output That's why the 24-loop delay is greater than the 26-th circuit. The researchers later were able to implement a new kind of transistor using transistor gates as transistors. The low power and high latency of this type of transistor made the designers select this type of transistor as a technology suitable for CMOS technology.

III. SYSTEM MODEL

Capacitors and resistors are considered to be destructive elements in the design of circuits and cause the amount of power consumed to be reduced to the product of these two values, and in general, all of the circuit parameters of the optimal state, so it is better to Do not use these two elements as much as possible. In this paper, a whole new collector is presented using silicon transistors. We used 16 transistors in this design.

Figure 1 shows the circuit of the proposed collector at the transistor level.

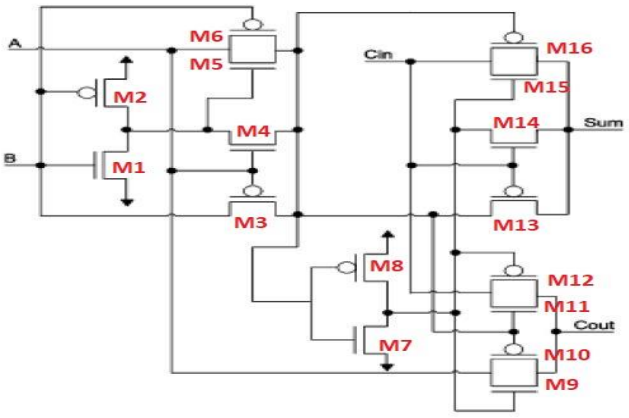

Fig .1 circuit of the proposed collector at the transistor level.

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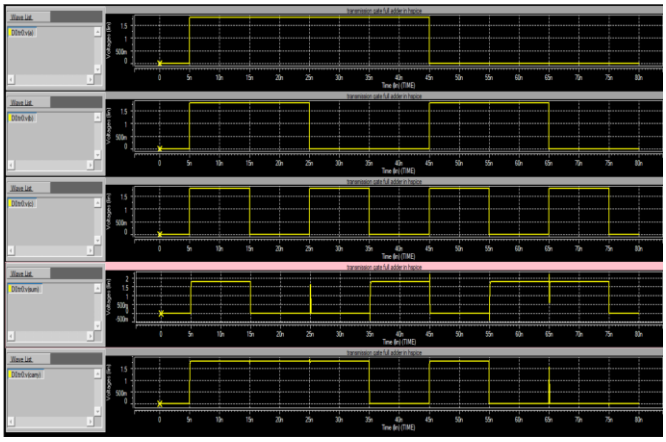

Fig.2 input and output of the proposed circuit

Figure 2 shows the input and output of the proposed circuit. Simulation results are calculated using HSPICE software

In Table 1, the simulation results of this complete collector are compared with the Conventional FA and Bridge FA examples.

Designs	Power	Delay	PDP
Conventional FA	**5.23E-07**	**7.97E-11**	**4.17E-17**
Bridge FA	**4.71E-07**	**8.82E-11**	**4.15E17**
Proposed Design	**7.12E-07**	**7.51E11**	**5.35E-17**

Table (1) simulation results(power,delay,pdp)

IV. INPUTS AND CIRCUIT OUTINGS

The simulation of the proposed scheme at 1.8 volts using the HSPICE software is shown in Fig. 2 to illustrate the functionality of the output. Examples of input and output waveforms are shown in Fig.2.
Where (A, B, C) are referred to as circuit inputs (SUM, Cout) as circuit outputs. As you can see in Figure 2, the output of the designed circuit is completely FULL-SWING, which means that the output is close to zero and one logic. One of the other reasons for FULL SWING is the presence of an overhead circuit that does not use elements such as capacitors and resistors that are considered to be destructive elements in designs.

V. CONCLUSION

capacitors and resistors of destructive elements in circuit design Accounts come in and cause the amount of power consumed, the delay, and the sum of these two values in total Ordinary parameters are eliminated from the optimal state, so it is preferable not to use these two elements in design as much as possible.
In this paper, we also show that the use of the gateway significantly improves the output parameters of the circuit.
Simulation of the proposed scheme at 1.8 Voltage with 3 inputs using the HSPICE software and we obtained the results.
. By examining the results we concluded that the proposed schemes compared to the previous designs in terms of parameters Latency is better.

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